1. JY-7133 Specifications

1.1 Overview

JY-7133 series modules are multi-function isolated digital I/O module, which can provide 64 channels of DI (64 Sinking/Sourcing Inputs, Bank-Isolated) or 8 channels of counter, supporting counting, frequency measurement, encoder and other functions.
Industrial DIO modules, like the JY-7133 series, are ideal for motor, valve control and automation control.

Please download the <JYPEDIA>, you can quickly inquire the product prices, the key features and available accessories.

1.2 Main Features

- DI：
  - 64 channels DI, ±60 V DC
  - Support Sourcing and Sinking input mode
  - Input Voltage:
    logic H:±2~±60V
    logic L:0~±1V
- Counter：
  - High operating voltage counter up to 60V
  - Up to 100 MHz internal clock rate
  - Counter Functions：
    Edge counting / Frequency measurement /Period measurement / Two-Edge separation/Quadrature/(x1/x2/x4) encoder/Two-Pulse encoder

1.3 Hardware Specifications

1.3.1 Isolated Digital Input

Number of Channel	64DI
Ground reference	GND
Input Voltage	Maximum input voltage:±60 VDC Input logic low voltage (VIL): 0~±1 VDC Input logic high voltage (VIH): ±2~±60 VDC
Input Type	Sourcing/Sinking
Common-mode Isolation	60 VDC (bank to bank)

Level	Min	Max
Input logic low voltage (VIL)	0 VDC	±1 VDC
Input logic high voltage (VIH)	±2 VDC	±60 VDC

Table 1 Isolated Digital Input

±2V inputs:±1.27mA,typical
±60V inputs: ±3.43mA,typical

Table 2 Input Current

1.3.2 Counter Specifications

Number of counters	8
Resolution	32 bits
Internal Clock Rate	100 MHz
Counter Input Functions	Edge counting Period measurement Frequency measurement Two-edge separation measurement Quadrature(×1/×2/×4) encoder Two-pulse encoder
Counter Input Frequency	10KHz(High Level ≤70us)
Counter Input Signal	Gate(Z) Source(A) Aux(B)

Table 3 Counter Specifications

1.3.3 External Digital Trigger

Trigger functions	Trigger source	PXI_TRIG<0..7> PFI_In<0..63>
	Polarity	Rising Edge/Falling Edge
	Counter /Timer functions	Start trigger
Module to module Trigger bus	Input source	PXI_TRIG<0..7>
	Output destination	PXI_TRIG<0..7>

Table 4 External Digital Trigger

1.3.4 Bus Interface

Bus interface	PXIe standard	x4 PXI Express peripheral module Specification V1.0 compliant
	Slot supported	x1 and x4 PXI Express or PXI Express hybrid slots

Table 5 Bus Interface

1.3.5 Physical Size

Dimensions	3U PXIe
Weight（TBD）	213.6 g

Table 6 Physical Size

1.3.6 Operating Environment

Ambient temperature range	0℃~50℃
Relative humidity range	20% to 80%, none-condensing

Table 7 Operating Environment

1.3.7 Storage Environment

Ambient temperature range	-20 °C to 50 °C
Relative humidity range	10% to 90%, none-condensing

Table 8 Storage Environment

Table of Contents

2. Introduction

This chapter presents the information how to use this manual and quick start if you are already familiar with Microsoft Visual Studio and C# programming language.

2.1 Abbreviations

DI: Digital Input

CI: Counter Input

DAQ: Data AcQuisition

PFI: Programmable Function Interface

2.2 Learn by Example

JYTEK has added **Learn by Example** in this manual. We provide many sample programs for this device. Please download and install the sample programs for this device. You can download a JYPEDIA excel file from our web www.jytek.com. Open JYPEDIA and search for JY-7133 in the driver sheet, select **JY7133.Examples.zip**. This will lead you to download the sample program for this device. In addition to the download information, JYPEDIA also has a lot of other valuable information, JYTEK highly recommend you use this file to obtain information from JYTEK.

Drivers	Update Date	Category	Support Module
JY7133_V1.0.0_Win.rar	2025/6/13	Driver	7133
JY7133_V1.0.0_Linux.tar.gz	2025/6/13	Driver	7133
JY7133_V1.0.0_Examples.rar	2025/6/13	Example	7133
JY7133_V1.0.0_C++Examples.rar	2025/6/13	Driver	7133
JY7133_V1.0.0_Python.rar	2025/6/13	Driver	7133
JY7133_V1.0.0_PythonExamples.rar	2025/6/13	Example	7133

Figure 1 JYPEDIA Information

In a **Learn by Example** section, the sample program is in bold style such as **Edge Counting**; the property name in the sample program is also in bold style such as **CIMode.Single**; the technical names used in the manual is in italic style such as *Pause trigger*. You can easily relate the property names in the example program with the manual documentation.

In an **Learn by Example** section, the experiment is set up as follow. A JY-7133 card is plugged in a desktop computer. The JY-7133 is connected to a DIN-100 terminal block. A signal source is also connected to the same terminal block.

The DIN-100 has 4 terminal columns, J1 – J4. In the rest of this manual, the wire connection in each **Learn by Example** section will be given by the pin numbers only.

3. Hardware Specifications

3.1 System Diagram

The system block diagram of JY-7133 series is shown in Figure 2.

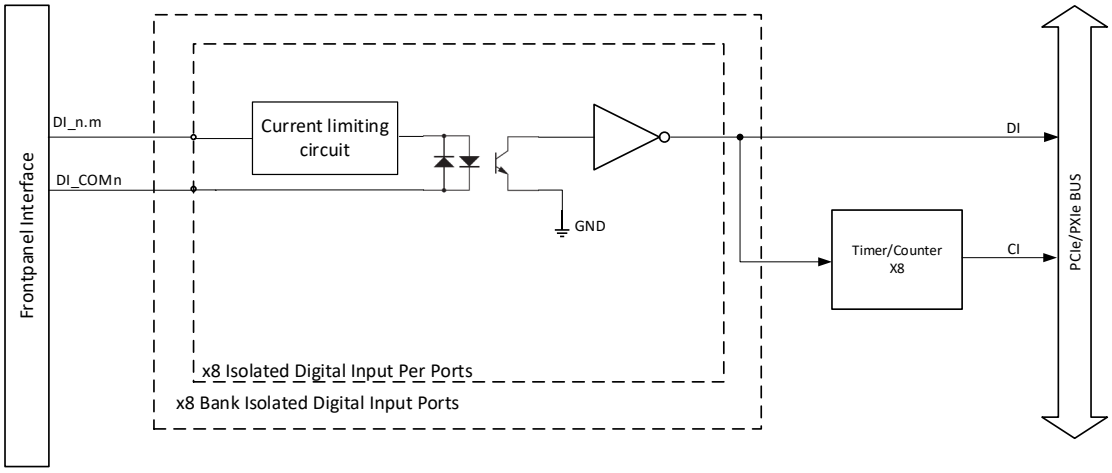

Figure 2 JY-7133 Series System Block Diagram

3.2 Front Panel and Pin Definition

Figure 3 Front Pannel

Pin Number	Signal	Pin Number	Signal
1	DI_0.0 /PFI_In_0	51	DI_1.0 /PFI_In_8
2	DI_0.1 /PFI_In_1	52	DI_1.1 /PFI_In_9
3	DI_0.2 /PFI_In_2	53	DI_1.2 /PFI_In_10
4	DI_0.3 /PFI_In_3	54	DI_1.3 /PFI_In_11
5	DI_0.4 /PFI_In_4	55	DI_1.4 /PFI_In_12
6	DI_0.5 /PFI_In_5	56	DI_1.5 /PFI_In_13
7	DI_0.6 /PFI_In_6	57	DI_1.6 /PFI_In_14
8	DI_0.7 /PFI_In_7	58	DI_1.7 /PFI_In_15
9	DI_COM0	59	DI_COM1
10	DI_COM0	60	DI_COM1
11	DI_COM0	61	DI_COM1
12	DI_COM0	62	DI_COM1
13	DI_2.0 /PFI_In_16	63	DI_3.0 /PFI_In_24
14	DI_2.1 /PFI_In_17	64	DI_3.1 /PFI_In_25
15	DI_2.2 /PFI_In_18	65	DI_3.2 /PFI_In_26
16	DI_2.3 /PFI_In_19	66	DI_3.3 /PFI_In_27
17	DI_2.4 /PFI_In_20	67	DI_3.4 /PFI_In_28
18	DI_2.5 /PFI_In_21	68	DI_3.5 /PFI_In_29
19	DI_2.6 /PFI_In_22	69	DI_3.6 /PFI_In_30
20	DI_2.7 /PFI_In_23	70	DI_3.7 /PFI_In_31
21	DI_COM2	71	DI_COM3
22	DI_COM2	72	DI_COM3
23	DI_COM2	73	DI_COM3
24	DI_COM2	74	DI_COM3
25	NC	75	NC
26	DI_4.0 /PFI_In_32	76	DI_5.0 /PFI_In_40
27	DI_4.1 /PFI_In_33	77	DI_5.1 /PFI_In_41
28	DI_4.2 /PFI_In_34	78	DI_5.2 /PFI_In_42
29	DI_4.3 /PFI_In_35	79	DI_5.3 /PFI_In_43
30	DI_4.4 /PFI_In_36	80	DI_5.4 /PFI_In_44
31	DI_4.5 /PFI_In_37	81	DI_5.5 /PFI_In_45
32	DI_4.6 /PFI_In_38	82	DI_5.6 /PFI_In_46
33	DI_4.7 /PFI_In_39	83	DI_5.7 /PFI_In_47
34	DI_COM4	84	DI_COM5
35	DI_COM4	85	DI_COM5
36	DI_COM4	86	DI_COM5
37	DI_COM4	87	DI_COM5
38	DI_6.0 /PFI_In_48	88	DI_7.0 /PFI_In_56
39	DI_6.1 /PFI_In_49	89	DI_7.1 /PFI_In_57
40	DI_6.2 /PFI_In_50	90	DI_7.2 /PFI_In_58
41	DI_6.3 /PFI_In_51	91	DI_7.3 /PFI_In_59
42	DI_6.4 /PFI_In_52	92	DI_7.4 /PFI_In_60
43	DI_6.5 /PFI_In_53	93	DI_7.5 /PFI_In_61
44	DI_6.6 /PFI_In_54	94	DI_7.6 /PFI_In_62
45	DI_6.7 /PFI_In_55	95	DI_7.7 /PFI_In_63
46	DI_COM6	96	DI_COM7
47	DI_COM6	97	DI_COM7
48	DI_COM6	98	DI_COM7
49	DI_COM6	99	DI_COM7
50	NC	100	NC

Table 9 Pin Definition

3.3 Default Routing for Counter Input/Output Signals

All counter input and output terminals are routed to a certain PFI by default as shown in Table 10 and Table 11

Functions	Signal Type	Ctr0	Ctr1	Ctr2	Ctr3
Edge Counting	Signal To Measure(Source)	PFI_In_0 (1)	PFI_In_8 (51)	PFI_In_16 (13)	PFI_In_24 (63)
	Pause Trigger(Gate)	PFI_In_1 (2)	PFI_In_9 (52)	PFI_In_17 (14)	PFI_In_25 (64)
	Count Direction(Aux)	PFI_In_2 (3)	PFI_In_10 (53)	PFI_In_18 (15)	PFI_In_26 (65)
Frequency Measurement	Signal To Measure(Gate)	PFI_In_1 (2)	PFI_In_9 (52)	PFI_In_17 (14)	PFI_In_25 (64)
Period Measurement	Signal To Measure(Gate)	PFI_In_1 (2)	PFI_In_9 (52)	PFI_In_17 (14)	PFI_In_25 (64)
Two-Edge Separation Measurement	First Signal to Measure(Gate)	PFI_In_1 (2)	PFI_In_9 (52)	PFI_In_17 (14)	PFI_In_25 (64)
	Second Signal to Measure(Aux)	PFI_In_2 (3)	PFI_In_10 (53)	PFI_In_18 (15)	PFI_In_26 (65)
Quadrature Encoder	A Signal(Source)	PFI_In_0 (1)	PFI_In_8 (51)	PFI_In_16 (13)	PFI_In_24 (63)
	B Signal(Aux)	PFI_In_2 (3)	PFI_In_10 (53)	PFI_In_18 (15)	PFI_In_26 (65)
	Z Signal(Gate)	PFI_In_1 (2)	PFI_In_9 (52)	PFI_In_17 (14)	PFI_In_25 (64)
Two-Pulse Encoder	A Signal(Source)	PFI_In_0 (1)	PFI_In_8 (51)	PFI_In_16 (13)	PFI_In_24 (63)
	B Signal(Aux)	PFI_In_2 (3)	PFI_In_10 (53)	PFI_In_18 (15)	PFI_In_26 (65)

Column "Ctr0" to "Ctr3": Pin Number is shown in (*).

Table 10 Counter Input Default Routing 1

Functions	Signal Type	Ctr4	Ctr5	Ctr6	Ctr7
Edge Counting	Signal To Measure(Source)	PFI_In_32(26)	PFI_In_40(76)	PFI_In_48(38)	PFI_In_56 (88)
	Pause Trigger(Gate)	PFI_In_33(27)	PFI_In_41(77)	PFI_In_49(39)	PFI_In_57 (89)
	Count Direction(Aux)	PFI_In_34(28)	PFI_In_42(78)	PFI_In_50(40)	PFI_In_58 (90)
Frequency Measurement	Signal To Measure(Gate)	PFI_In_33(27)	PFI_In_41(77)	PFI_In_49(39)	PFI_In_57 (89)
Period Measurement	Signal To Measure(Gate)	PFI_In_33(27)	PFI_In_41(77)	PFI_In_49(39)	PFI_In_57 (89)
Two-Edge Separation Measurement	First Signal to Measure(Gate)	PFI_In_33(27)	PFI_In_41(77)	PFI_In_49(39)	PFI_In_57 (89)
	Second Signal to Measure(Aux)	PFI_In_34(28)	PFI_In_42(78)	PFI_In_50(40)	PFI_In_58 (90)
Quadrature Encoder	A Signal(Source)	PFI_In_32(26)	PFI_In_40(76)	PFI_In_48(38)	PFI_In_56 (88)
	B Signal(Aux)	PFI_In_34(28)	PFI_In_42(78)	PFI_In_50(40)	PFI_In_58 (90)
	Z Signal(Gate)	PFI_In_33(27)	PFI_In_41(77)	PFI_In_49(39)	PFI_In_57 (89)
Two-Pulse Encoder	A Signal(Source)	PFI_In_32(26)	PFI_In_40(76)	PFI_In_48(38)	PFI_In_56 (88)
	B Signal(Aux)	PFI_In_34(28)	PFI_In_42(78)	PFI_In_50(40)	PFI_In_58 (90)

Column "Ctr4" to "Ctr7": Pin Number is shown in (*).

Table 11 Counter Input Default Routing 2

4. Order Information

- PXIe-7133 (PN: JY8628450-01)

64-Channel, 60 VDC, Sink/Source Inputs,8-CH Counter/Timer Bank-Isolated PXIe Multifunction Digital Input Module

- Accessories:

Cable:

ACL-1020100-1 1M 100pin SCSI twisted pair cable (PN: JY4910923-01)

ACL-1020100-2 2M 100pin SCSI twisted pair cable (PN: JY7155665-01)

Terminal Block:

DIN-100-1 100-Pin SCSI Terminal block (PN: JY7739162-01)

5. Software

5.1 System Requirements

JY-7133 modules can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

Linux Version
Ubuntu LTS
16.04： 4.4.0-21-generic(desktop/server)
16.04.6：4.15.0-45-generic(desktop) 4.4.0-142-generic(server)
18.04： 4.15.0-20-generic(desktop) 4.15.0-91-generic(server)
18.04.4：5.3.0-28-generic (desktop) 4.15.0-91-generic(server)
Localized Chinese Version
中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）: 3.10.0-862.9.1.nd7.zx.18.x86_64
中标麒麟高级服务器操作系统软件V7.0U6: 3.10.0-957.el7.x86_64

Table 12 Supported Linux Versions

5.2 System Software

When using the JY-7133 in the Window environment, you need to install the following software from Microsoft website:

Microsoft Visual Studio Version 2015 or above,

.NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the resources limitation, JYTEK only tested JY-7133 with .NET Framework 4.0 with Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

5.3 C# Programming Language

All JYTEK default programming language is Microsoft C#. This is Microsoft recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross platform programming language.

5.4 JY-7133 Series Hardware Driver

After installing the required application development environment as described above, you need to install the JY-7133 hardware driver.

JYTEK hardware driver has two parts: the shared common driver kernel software (FirmDrive) and the specific hardware driver.

Common Driver Kernel Software (FirmDrive): FirmDrive is the JYTEK's kernel software for all hardware products of JYTEK instruments. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

Specific Hardware Driver: Each JYTEK hardware has a C# specific hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various JY-7133 function. JYTEK has standardized the ways which JYTEK and other vendor's DAQ boards are used by providing a consistent user interface, using the methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ module works, you should be able to know how to use all other DAQ hardware by using the same methods.

5.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use JY-7133 boards, you need to install a set of free C# utilities, SeeSharpTools from JYTEK. The SeeSharpTools offers rich user interface functions you will find convenient in developing your applications. They are also needed to run the examples come with JY-7133 hardware. Please register and down load the latest SeeSharpTools from our website, www.jytek.com.

5.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# applications in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop environment. This is JYTEK recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

6. Operating JY-7133

This chapter provides the operation guides for JY-7133, including Timer and programmable I/O interface, etc.

JYTEK provides extensive examples, on-line help and documentation to assist you to use the JY-7133 module. JYTEK strongly recommends you go through these examples before writing your own application. In many cases, an example can also be a good starting point for a user application.

6.1 Quick Start

After you have installed the driver software and the SeeSharpTools, you are ready to use Microsoft Visual Studio C# to operate the JY-7133 products.

If you are already familiar with Microsoft Visual Studio C#, the quickest way to use JY-7133 boards is to go through our extensive examples. We provide source code of our examples. In many cases, you can modify the source code and start to write your applications.

6.2 Digital I/O Operations

The JY-7133 provides 64 channels of isolated digital input.

6.2.1 Digital Input Connection Guide

The JY-7133 device supports 64 channels of isolated digital input. Here's a guide to connect an input signal to a channel.

- **Sinking Configuration**

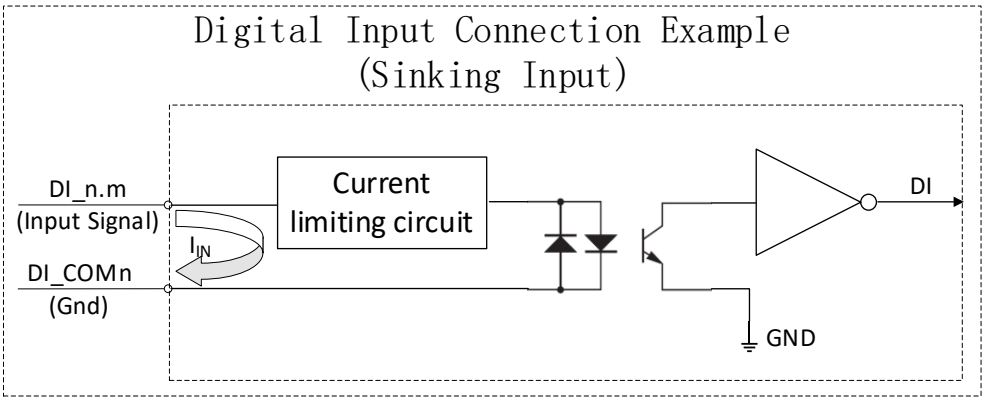

Figure 4 Digital Input Connection Example（Sinking Input）

1. **Identify the Input Terminal:** Locate the input channel on the device you intend to use, typically labeled as DI_n.m where “n” represents the port number and “m” represents the line number.
2. **Connect the Input Signal:** Connect the positive input signal to the input terminal (DI_n.m) of the module.
3. **Connect the COM:** Connect the ground of your signal source to the COM terminal

(DI_COMn) of the module.

4. **Operation:** Applying a DC voltage of at least 2 V across the two input terminals (DI_n.m and DI_COMn) represents a logic high for that input.
    - If no voltage is present (a voltage of 1 V or less), the module represents a logic low for that input.
    - DC voltages between 1 V and 2 V are invalid and represent an unreliable value.

● Sourcing Configuration

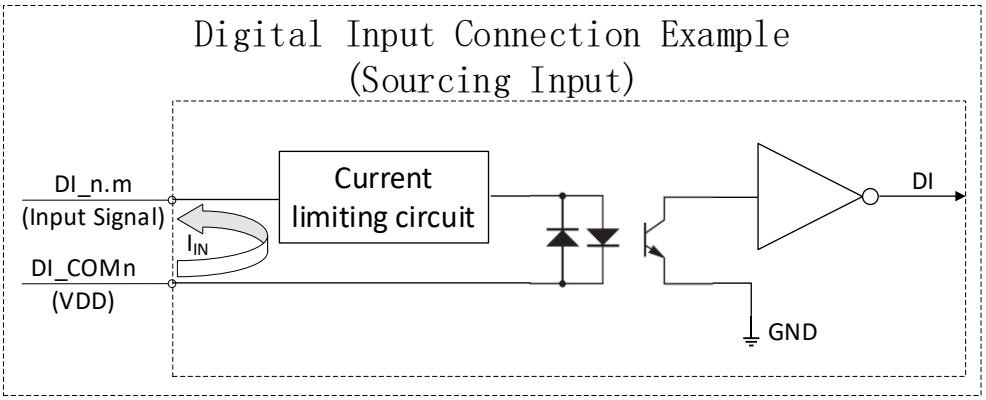

Figure 5 Digital Input Connection Example（Sourcing Input）

1. **Identify the Input Terminal:** Locate the input channel on the device you intend to use, typically labeled as DI_n.m where “n” represents the port number and “m” represents the line number.
2. **Connect the Input Signal:** Connect the negative input signal to the input terminal (DI_n.m) of the module.
3. **Connect the COM:** Connect the VDD of your signal source to the COM terminal (DI_COMn) of the module.
4. **Operation:** Applying a DC voltage of at least 2 V across the two input terminals (DI_n.m and DI_COMn) represents a logic high for that input.
    - If no voltage is present (a voltage of 1 V or less), the module represents a logic low for that input.
    - DC voltages between 1 V and 2 V are invalid and represent an unreliable value.

6.3 Counter Measurement Operations

The JY-7133 has eight identical 32-bit channels of timer/counter as shown in Figure 6.

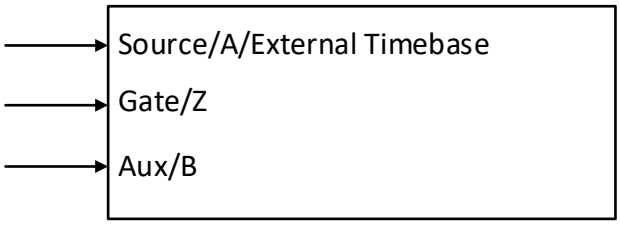

Figure 6 Counter Input Diagram

Each counter has eight input terminals and one output terminal, and these terminals have different functions in different counter measurement application described below:

- Edge Counting
- Frequency Measurement
- Period Measurement
- Two-Edge Separation Measurement
- Quadrature Encoder (x1, x2, x4)
- Two-Pulse Encoder

6.3.1 Edge Counting

The counter counts the number of active edges of input signal. Default, the input signal must be connected to Counter Source terminal.

Set JY7133CITask.Type to CIType.EdgeCounting to use this function.

Timing

1) Single Mode

The counting value is written to the register on each rising edge or falling edge of the measured signal as shown in Figure 7.

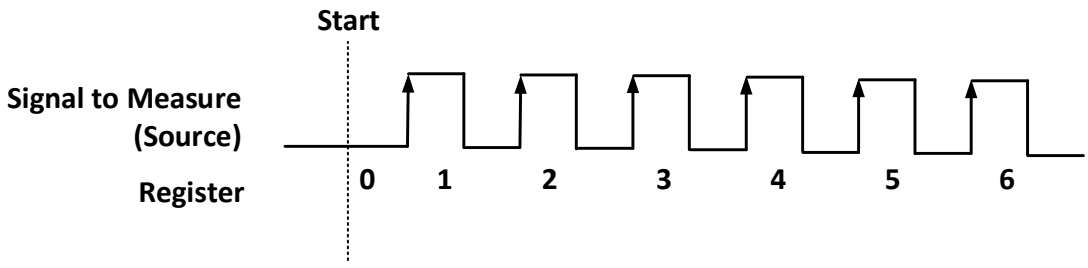

Figure 7 Simple Edge Counting in Single Mode

To configure the counter to work in this mode, set JY7133CITask.Mode to CIMode.Single.

Pause Trigger

Pause trigger is used to pause counting when the input signal is active depending on active polarity configuration as shown in Figure 8. Default, the Pause Trigger signal must be connected to Counter Gate terminal.

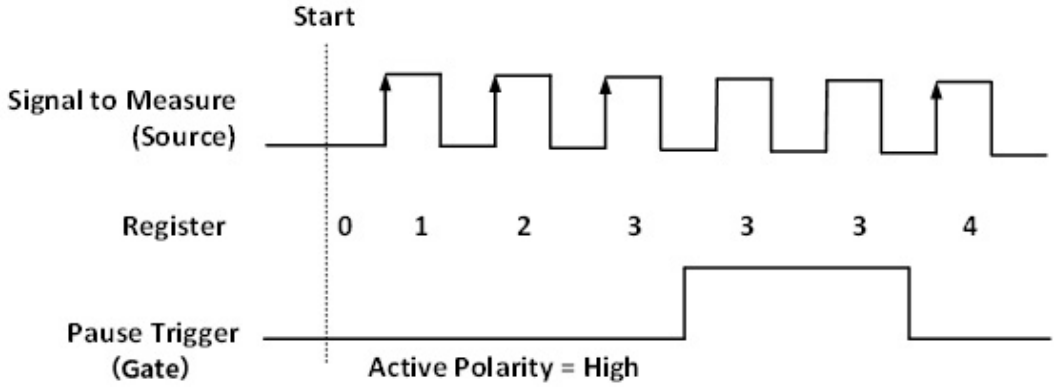

Figure 8 Pause Trigger

To configure the pause trigger, use the properties as below:

JY7133CITask.EdgeCounting.Pause.ActivePolarity – To set active level (high or low) to pause counting.

Count Direction

User can control the counting direction through software configuration or by an external input signal. Default, the external control direction signal must be connected to Counter Aux terminal.

When using an input signal to control the counting direction, the counter counts up when the signal is high and counts down when the signal is low as shown in Figure 9.

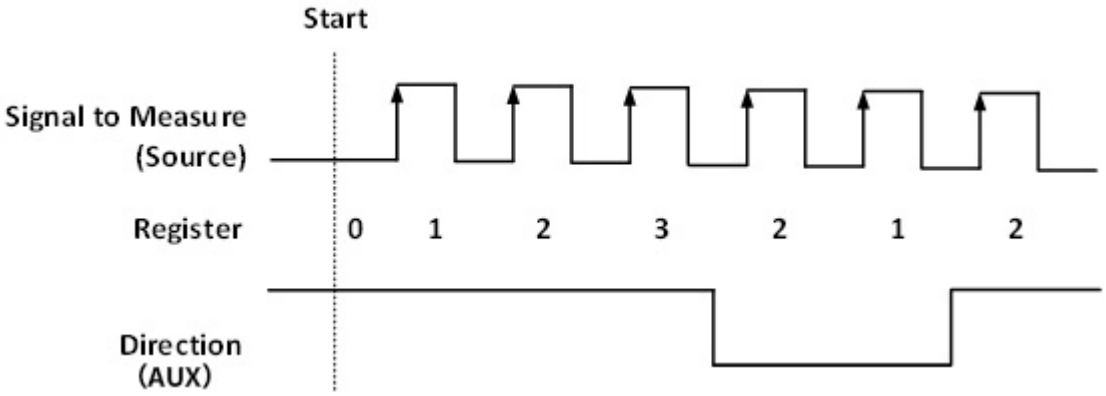

Figure 9 Count Direction

To configure the count direction, use the properties as below:

JY7133CITask.EdgeCounting.Direction – To specify count up, count down, or controlled by an external signal.

Exporting Count Event

When the counting value reaches the specified threshold, the counter will generate a pulse. To change the threshold, using following property:

JY7133CITask.EdgeCounting.OutEvent.Threshold

Terminals

To change the terminal of signals instead of using its default value as shown in chapter 3.2, using following properties:

JY7133CITask.EdgeCounting.InputTerminal – Signal-to-measure input terminal.

JY7133CITask.EdgeCounting.Pause.Terminal – Pause signal input terminal.

JY7133CITask.EdgeCounting.DirTerminal – External direction control signal input terminal.

JY7133CITask.EdgeCounting.OutEvent.Terminal – Count event output terminal.

6.3.2 Frequency Measurement

The counter measures the frequency of the signal. Default, the measured signal must be connected to Counter Gate terminal.

Set JY7133CITask.Type to CIType.Frequency to use this function.

Timing

1) Single Mode

Frequency Measurement without sample clock is actually using Pulse Width Measurement internally, refer to chapter for more information.

Every time the user reads the data, driver will automatically calculate the frequency (f_x) according to the HighTick ($tick_h$), LowTick ($tick_l$) values and known frequency of the timebase (f_{base}) according to the fomular and return the signal frequency to the user.

$$f_x = f_{base} \times \frac{1}{tick_h + tick_l}$$

To configure the counter to work in this mode, set JY7133CITask.Mode to CIMode.Single.

Timebase

By default, the counter uses the onboard 100MHz timebase to measure pulses. Use the property JY7133CITask.FrequencyMeas.Timebase to configure the timebase.

Please refer to chapter 6.4.2 for more information about timebase.

Terminals

To change the terminal of signals instead of using its default value shown in chapter 3.2, using following properties:

JY7133CITask.FrequencyMeas.InputTerminal – Signal-to-measure input terminal.

JY7133CITask. FrequencyMeas.Timebase.External.Terminal – External timebase input terminal.

6.3.3 Period Measurement

The counter measures the period of the signal. Default, the signal must be connected to Counter Gate terminal.

Set JY7133CITask.Type to CIType.Period to use this function.

Period Measurements is using Frequency Measurement internally and returns the reciprocal of Frequency Measurement. Refer to chapter for more information.

6.3.4 Two-Edge Separation

The counter measures the separation (interval between each rising edges of two signals) between the rising edges of two signals. Default, the first signal must be connected to Counter Gate terminal and the second signal must be connect to Counter Aux terminal.

Set JY7133CITask.Type to CIType.TwoEdgeSeparation to use this function.

Timing

1) Single Mode

The number of rising edges of timebase between the rising edge of the first signal and the rising edge of the second signal is written to the register on each rising edge of the second signal.

The number of rising edges of timebase between previous rising edge of the second signal and current rising edge of the first signal is written to the register on each rising edge of the first signal.

As shown in Figure 10.

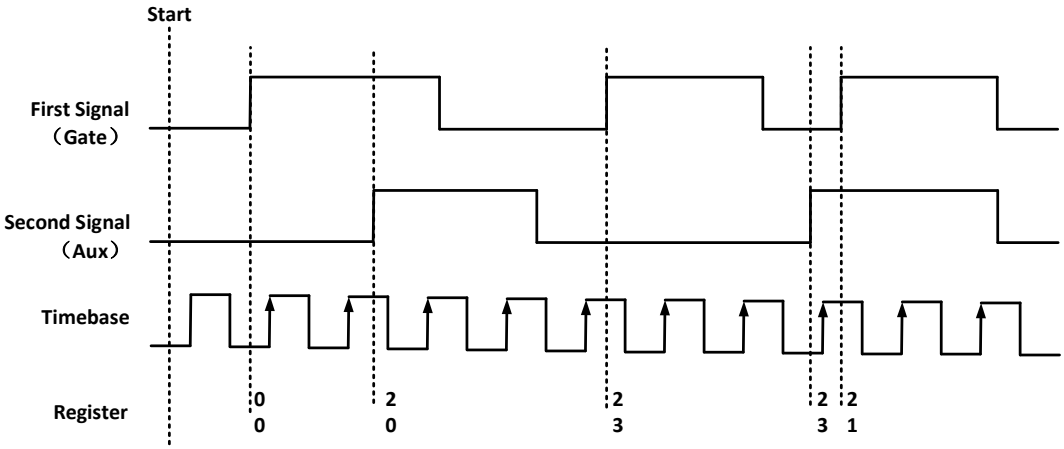

Figure 10 Two-Edge Separation in Single Mode

To configure the counter to work in this mode, set JY7133CITask.Mode to CIMode.Single.

Timebase

By default, the counter uses the onboard 100MHz timebase to measure pulses. Use the property JY7133CITask.TwoEdgeSeparation.Timebase to configure the timebase.

Please refer to chapter 6.4.2 for more information about timebase.

Terminals

To change the terminal of signals instead of using its default value shown in chapter 3.2, using following properties:

JY7133CITask.TwoEdgeSeparation.FirstInputTerminal – First signal-to-measure input terminal.

JY7133CITask.TwoEdgeSeparation.SecondInputTerminal – First signal-to-measure input terminal.

JY7133CITask.TwoEdgeSeparation.Timebase.External.Terminal – External timebase input terminal.

6.3.5 Quadrature Encoder

The quadrature encoder includes three encoding type: x1, x2, and x4.

Set JY7133CITask.Type to CIType. QuadEncoder to use this function, and use property JY7133CITask.QuadEncoder.EncodingType to change the type of encoding. Default, the A signal must be connected to Counter A terminal, the B signal must be connected to Counter B terminal and the Z signal must be connected to Counter Z terminal. For terminal Z, you can connect Z signal to it, or you can disable Z with property "ZReloadEnabled".

Encoding Type

1) x1 Encoding

When A signal leads B signal, the counter increases the count value on the rising edge of A signal; when B signal leads A signal, the counter decreases the count value on the falling edge of A signal as shown in Figure 11.

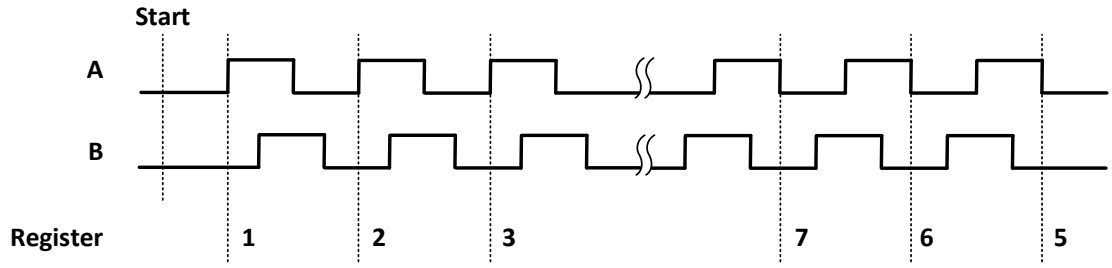

Figure 11 Quadrature Endcoder x1 Mode

2) x2 Encoding

When A signal leads B signal, the counter increases the count on the rising edge and the falling edge of A signal; when B signal leads A signal, the counter decreases the count value the rising edge and falling edge of A signal as shown in Figure 12.

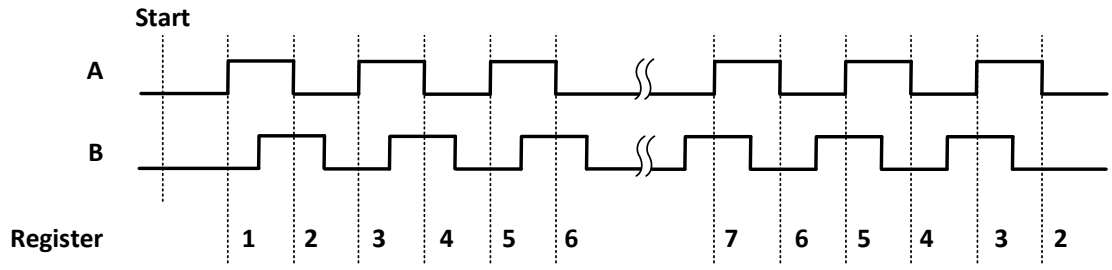

Figure 12 Quadrature Encoder x2 Mode

3) x4 Encoding

When A signal leads B signal, the counter increases the count value on the rising and falling edges of A signal and B signal. When B signal leads A signal, the counter decreases the count value on the rising and falling edges of A signal and B signal. As shown in Figure 13.

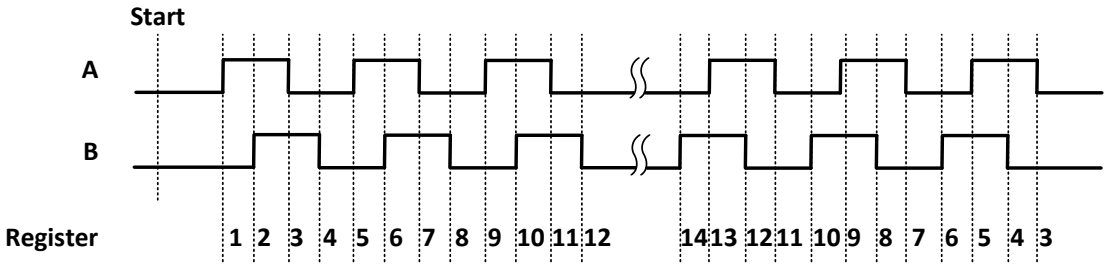

Figure 13 Quadrature Encoder x4 mode

Channel Z Behavior

The reload phase is when Z signal is high and A signal and B signal are low.

Timing

Take Encoding x1 mode as an example.

1) Single Mode

The count value is written to the register on each rising edge of the A signal, as shown in Figure 11.

To configure the counter to work in this mode, set JY7133CITask.Mode to CIMode.Single.

Terminals

To change the terminal of signals instead of using its default value as shown in chapter 3.2, use following properties:

JY7133CITask.QuadEncoder.AInputTerminal – Signal A input terminal.

JY7133CITask.QuadEncoder.ZInputTerminal – Signal Z input terminal.

JY7133CITask.QuadEncoder.BInputTerminal – Signal B input terminal.

6.3.6 Two-Pulse Encoder

The count value increases on the rising edge of A signal and decreases on the rising edge of B signal. Default, the A signal must be connected to Counter A terminal, the B signal must be connected to Counter B terminal.

Set JY7133CITask.Type to CIType.TwoPulseEncoder to use this function

Timing

1) Single Mode

The count value is written to the register on each rising edge of the A signal, and B signel, as shown in Figure 14.

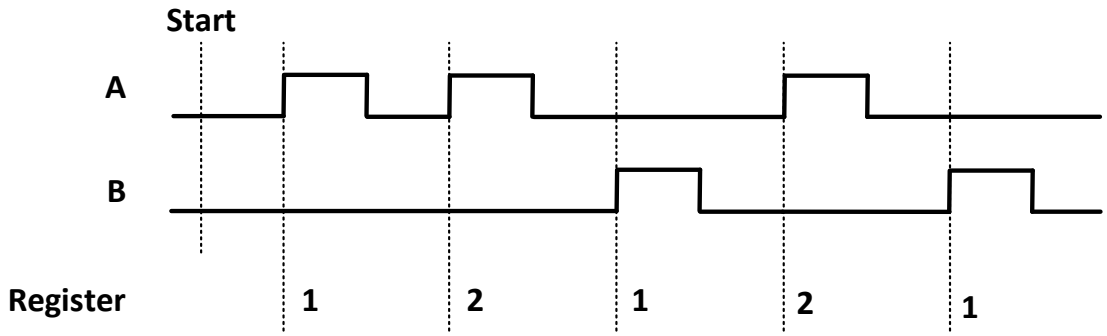

Figure 14 Two-Pulse Encoder in Single Mode

To configure the counter to work in this mode, set JY7133CITask.Mode to CIMode.Single.

Terminals

To change the terminal of signals instead of using its default value as shown in chapter 3.2, use following properties:

JY7133CITask.TwoPulseEncoder.AInputTerminal – Signal A input terminal.

JY7133CITask. TwoPulseEncoder.BInputTerminal – Signal B input terminal.

6.3.7 Counter Connection Guide

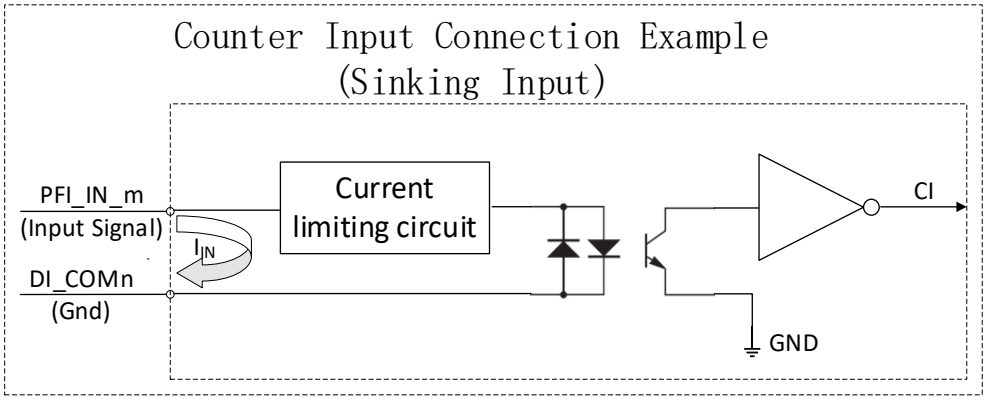

Figure 15 Counter Input Connection Example(Sinking Input)

1. **Signal Input Connection:** Connect the external input signal to PFI_IN_m (Input Signal), and its return path to DI_COMn (Gnd).
2. **Power Source Connection**: The module's internal circuit (current - limiting, optocoupler, etc.) uses internal power (e.g., related to Vcc).
3. **Common Ground Connect**: Connect DI_COMn (Gnd) to the module's GND for a unified ground.
4. Operation:
   - **Signal Present:** Current flows in the loop, drives the optocoupler (isolates & transmits), and the amplified signal outputs as CI.
   - **No Signal:** Insufficient current to activate the optocoupler; CI shows "no input" (e.g., low level).

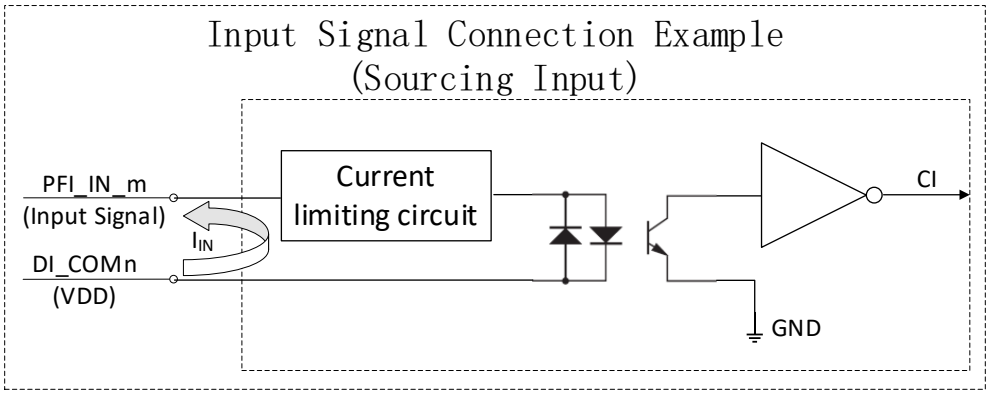

Figure 16 Counter Input Connection Example(Sourcing Input)

1. **Signal Input Connection:** Connect the input signal to PFI_IN_m (Input Signal), and the positive power (VDD) to DI_COMn (VDD).
2. **Power Source Connection:** DI_COMn (VDD) powers the internal circuit (current - limiting, optocoupler).
3. **Common Ground Connection:** Link the power source ground to the module's GND.
4. Operation:
   - **Signal Present:** Current flows, drives the optocoupler (isolates & transmits), and outputs as CI.
   - **No Signal:** Insufficient current; CI shows "no input" (e.g., low level).

6.4 Clocks

Figure 17 shows the structure of counter clock system.

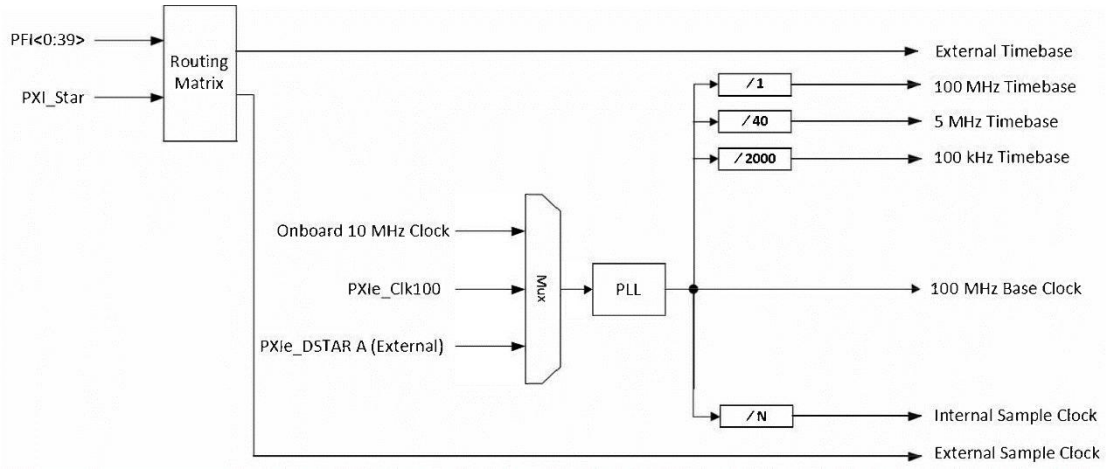

Figure 17 Clocks Diagram

6.4.1 PLL

PLL (Phase Locked Loop) is a phase-locked clock generator that can generate a clock signal of a specified frequency according to the selected reference clock source.

JY-7133 Series boards support the following reference clock source:

1) Onboard 10MHz Clock

Using the on-board 10MHz (TXCO) as the PLL input source can help improve the PLL output clock performance, including improving clock accuracy, temperature stability, and phase noise.

2) PXIe_CLK100

The PXIe_CLK00 signal is a 100MHz clock provided by the PXIe backplane for every peripheral slot. When using this clock, PXIe-7133 can provide multi-card synchronization.

3) External Reference Clock

An external reference clock is a clock provided by user through terminal PXIe-DSTARA. To use an external reference clock, the user needs to specify its frequency.

By default, onboard 10MHz Clock is selected as the reference clock source. To change the reference clock source, configure the device as follows:

Set property Task.Device.ReferenceClock.Source to target reference clock source. Task is user defined JY7133CITask.

If the target clock source is External:

- Set Task.Device.ReferenceClock.External.Terminal to desired terminal.
- Set Task.Device.ReferenceClock.External.Frequency to the frequency of this clock source.

Call method Device.Commit() to activate the configuration.

Note:

1. Clock configuration are not allowed to change while any counter tasks are running.

   Clock configuration is applied to all tasks (including DI, CI).

   The JY-7133 module must be powered off and restarted if the user submits the incorrect clock frequency by using external clock source (PXIe_DSTARA).

6.4.2 Timebase

JY7133 provides four options for timebase source as follows:

Internal 100MHz: - Same signal as the 100 MHz base clock generated by PLL.

Internal 5MHz – Generated by dividing down the 100 MHz timebase.

Internal 100kHz – Generated by dividing down the 100 MHz timebase.

6.5 Start Trigger

For all counter measurement and generation applications, the task starts running when the start trigger happens.

Start trigger has the following types:

Immediately

The task will start immediately after JY7133xxTask.Start() is called.

Software

After calling JY7133xxTask.Start () on the software, the task will not start until a software trigger is received.

Digital

An external digital trigger is generated when the external trigger source terminal detects a rising edge as shown in Figure 18.

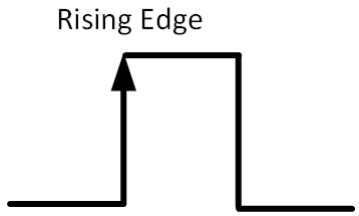

Figure 18 Rising Edge Digital Trigger

6.6 Multi-Card Synchronization

JY-7133 Series modules support master-slave synchronization mechanism to achieve multi-card synchronous acquisition.

Master-Slave Synchronization

It will use 3 signals, Reference clock, Sync Pulse and Triger to achieve data acquisition simultaneously with multiple modules. First, the master module will notice all of slave modules by routing the trigger signal through PXI trigger bus, PXI_TRIG<0..7> when master module receives trigger. Second, we also need to make sure every module to start the acquisition task in the same time, therefore we could take advantage of PXI system which can provide a synchronization pulse, PXIe_SYNC100 to coordinate with the acquisition task of multiple modules.

Third, every module must use the same reference clock to keep pace with each others and user can use PXIe_CLK100 which provides by PXI system as reference clock.

The timing diagram is shown as Figure 19.

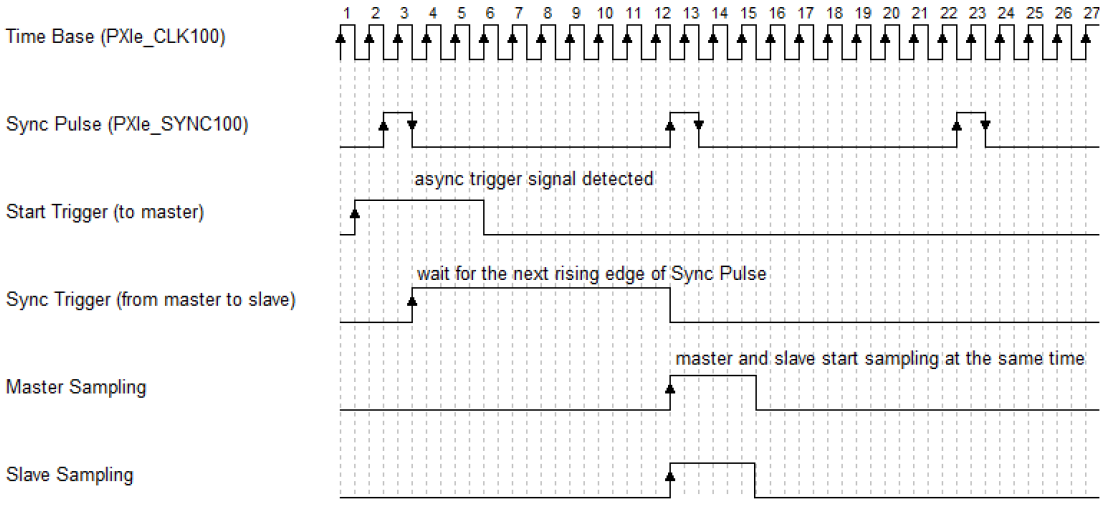

Figure 19 Master-Slave Synchronization

To enable the multi-card synchronization, configure the board as follows:

1. Set each task on different card as Master or Slave. Only one master is allowed.
2. Set the reference clock source of master card and slave card to PXIe_CLK100. Refer to 6.4.1 for more information.
3. Route trigger signals of all tasks to the same signal terminal, trigger signal will be sent from the master card to all slave cards through this terminal.
4. Route Sync Pulse signals of all tasks to the same signal terminal, Sync Pulse signals will be sent from the master card to all slave cards through this terminal.
5. Start all slave tasks.
6. Start the master task (if digital trigger or software trigger is enabled, you need to wait for the trigger signal to arrive), all the tasks will start to work synchronously on a rising edge of the PXIe_SYNC100 signal.

7. Using JY-7133 in Other Software

While JYTEK's default application platform is Visual Studio, the programming language is C#, we recognize there are other platforms that are either becoming very popular or have been widely used in the data acquisition applications. Among them are C++ etc. This chapter explains how you can use JY-7133 DAQ card using one of this software.

7.1 C++

JYTEK internally uses our C++drivers to design the C# drivers. We recommend our customers to use C# drivers because C# platform deliver much better efficiency and performance in most situations. We also make our C++ drivers available. However, due to the limit of our resources, we do not actively support C++ drivers. If you want to be our partner to support C++ drivers, please contact us.

8. About JYTEK

8.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company has evolved from re-branding and reselling PXI(e) and DAQ products to a fully-fledged product company. The company offers complete lines of PXI, DAQ, USB products. More importantly, JYTEK has been promoting open-sourced based ecosystem and offers complete software products. Presently, JYTEK is focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we also have R&D centers in Xi'an and Chongqing. We also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Guangdong, Haerbin, and Changchun. We also have many partners who provide system level support in various cities.

8.2 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

8.3 JYTEK Warranty and Support Services

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

9. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explanation for JYTEK JY-7133 Series family of multi-function data acquisition boards. The manual is copyrighted by JYTEK.

No warranty is given as to any implied warranties, express or implied, including any purpose or non-infringement of intellectual property rights, unless such disclaimer is legally invalid. JYTEK is not responsible for any incidental or consequential damages related to performance or use of this manual. The information contained in this manual is subject to change without notice.

While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

Shanghai Jianyi Technology Co., Ltd.

Address: Room 201, Building 3, NO.300 Fangchun Road, Shanghai.

Post Code: 201203

Tel: 021-5047 5899

Website: www.jytek.com